


P45K V10

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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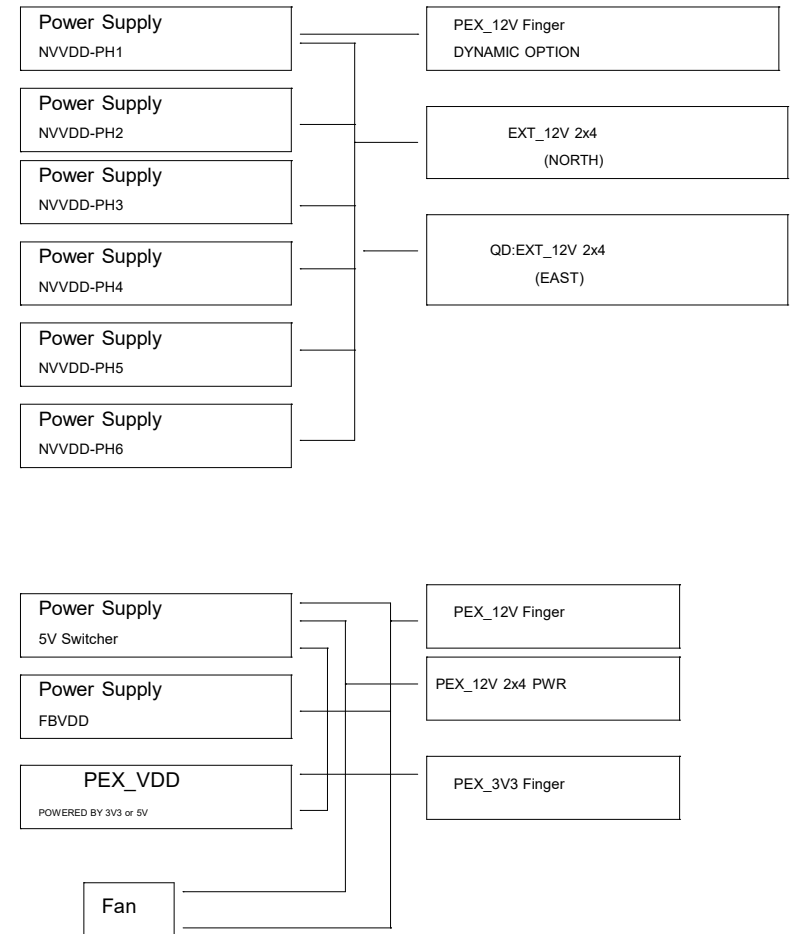
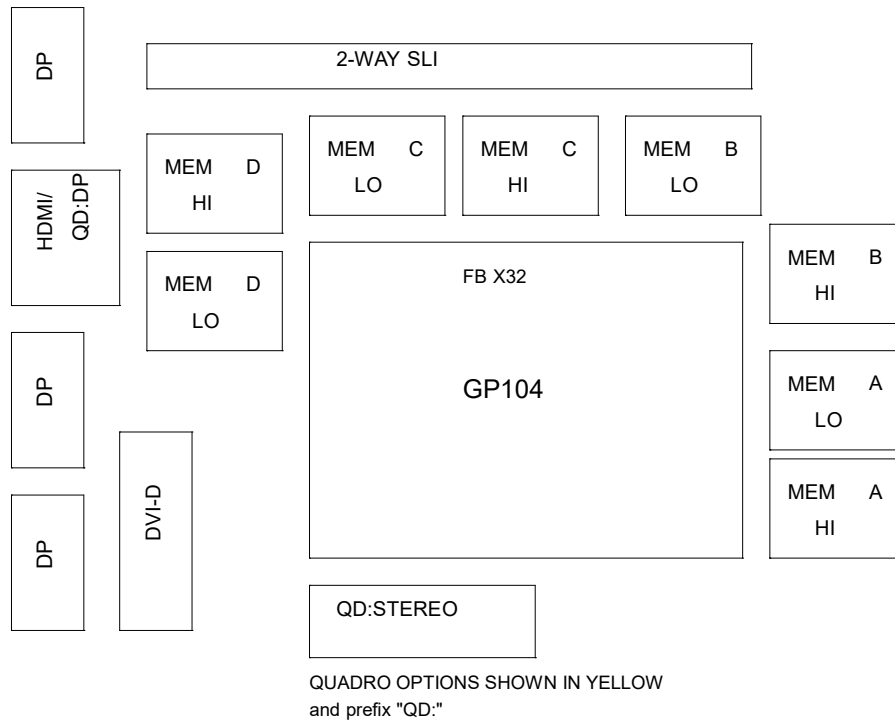
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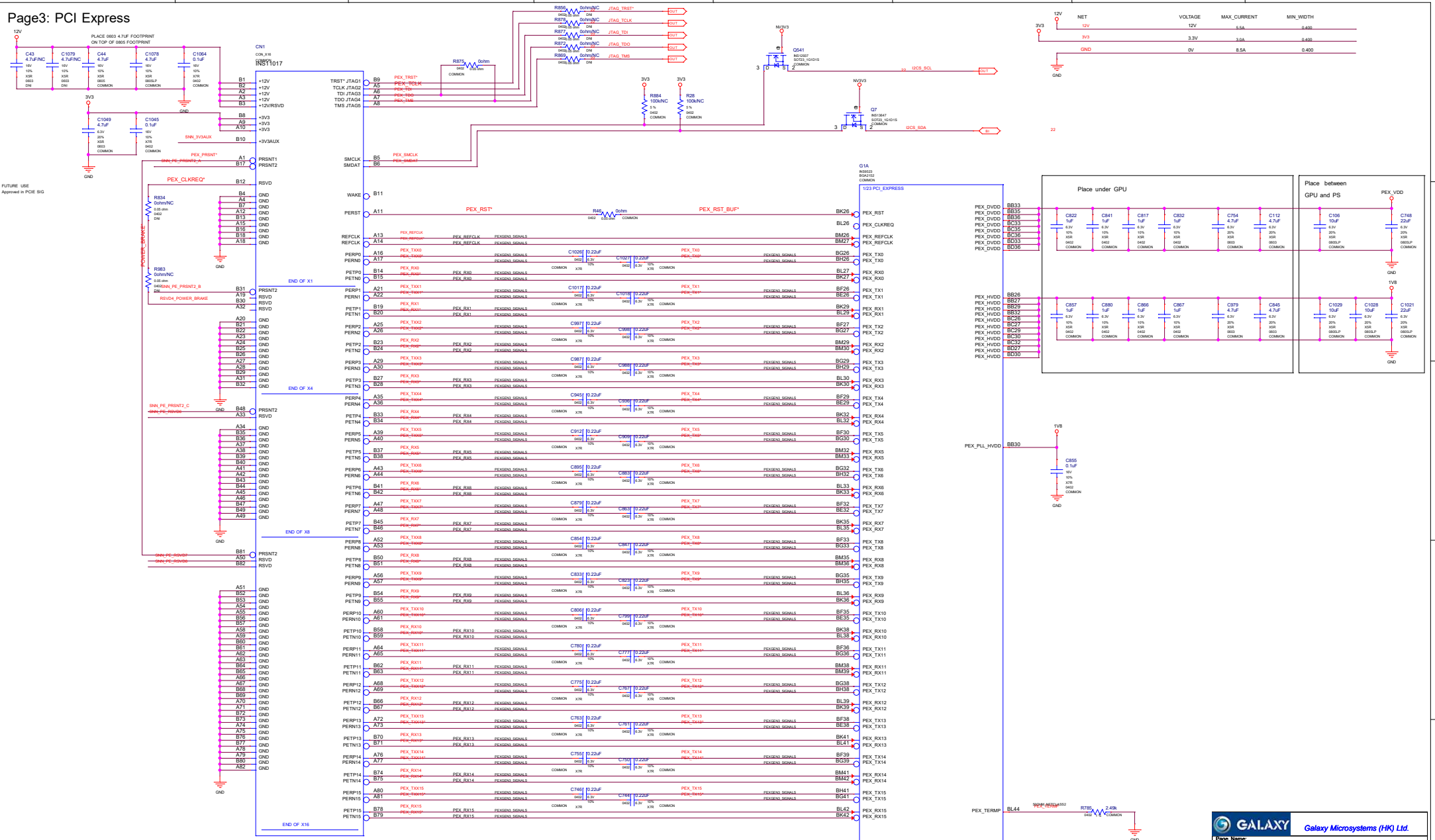
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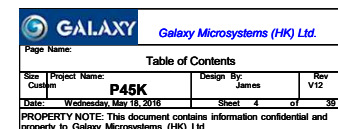
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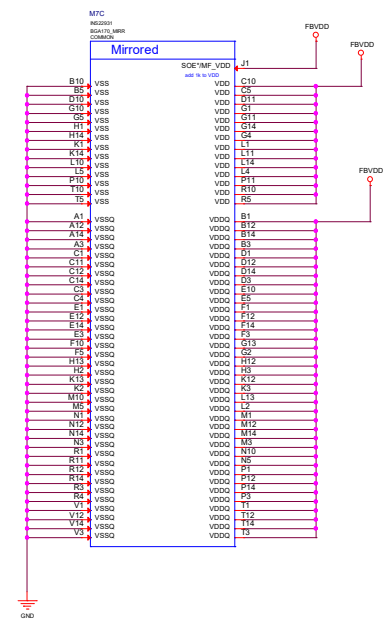



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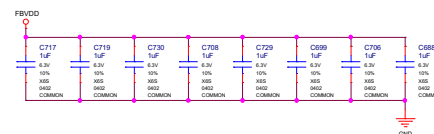
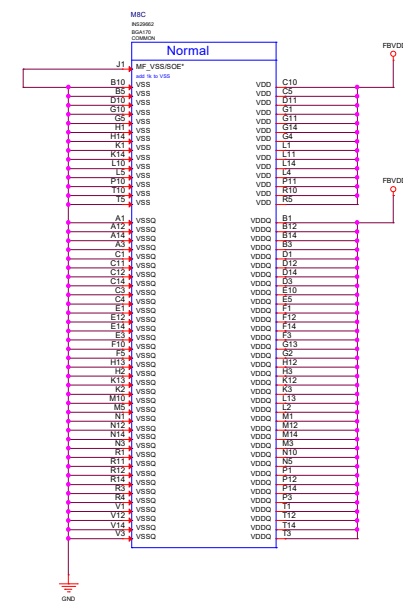
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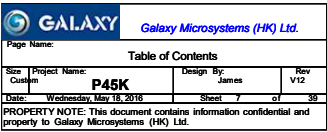
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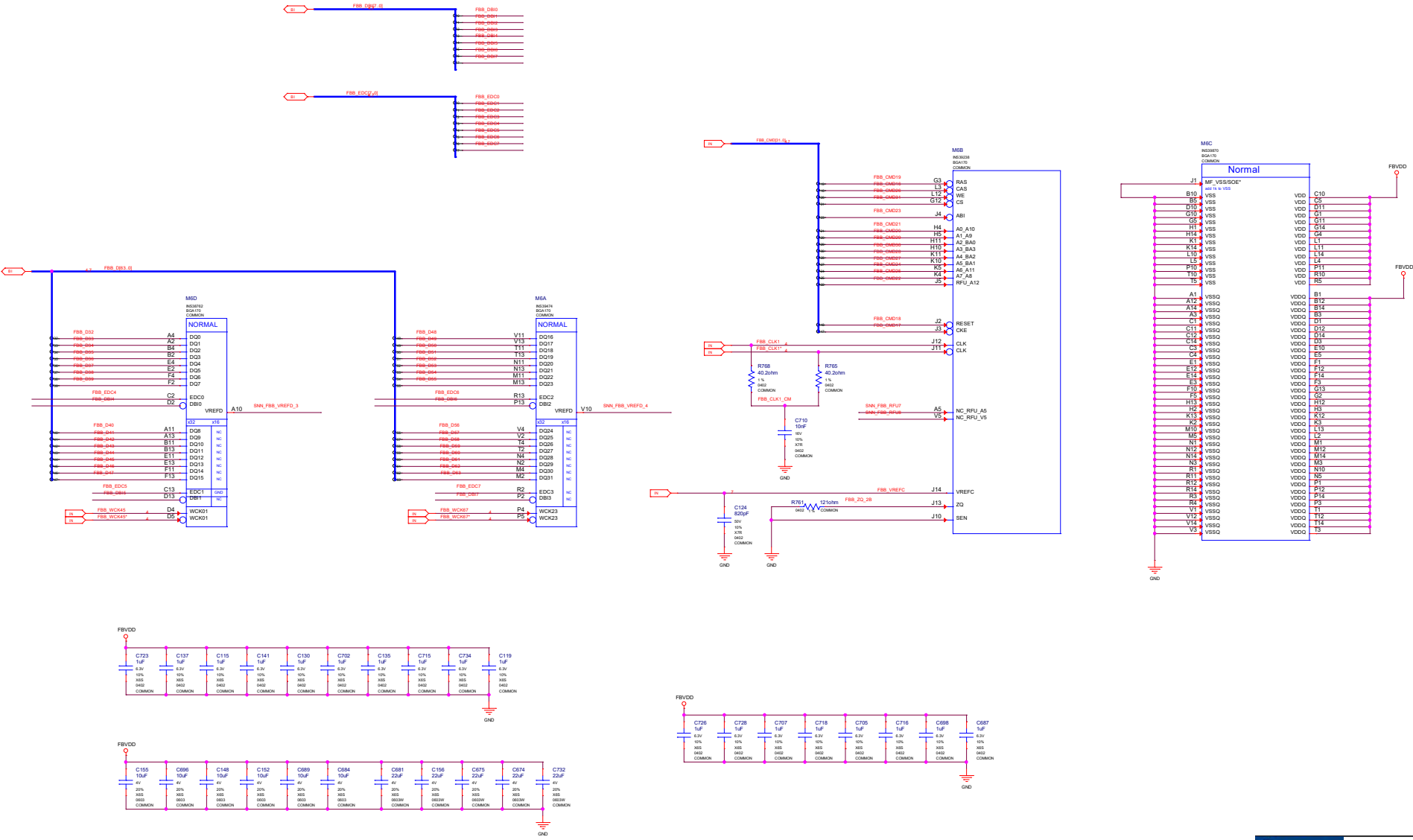
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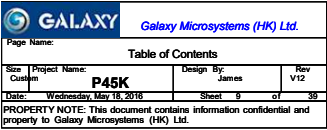


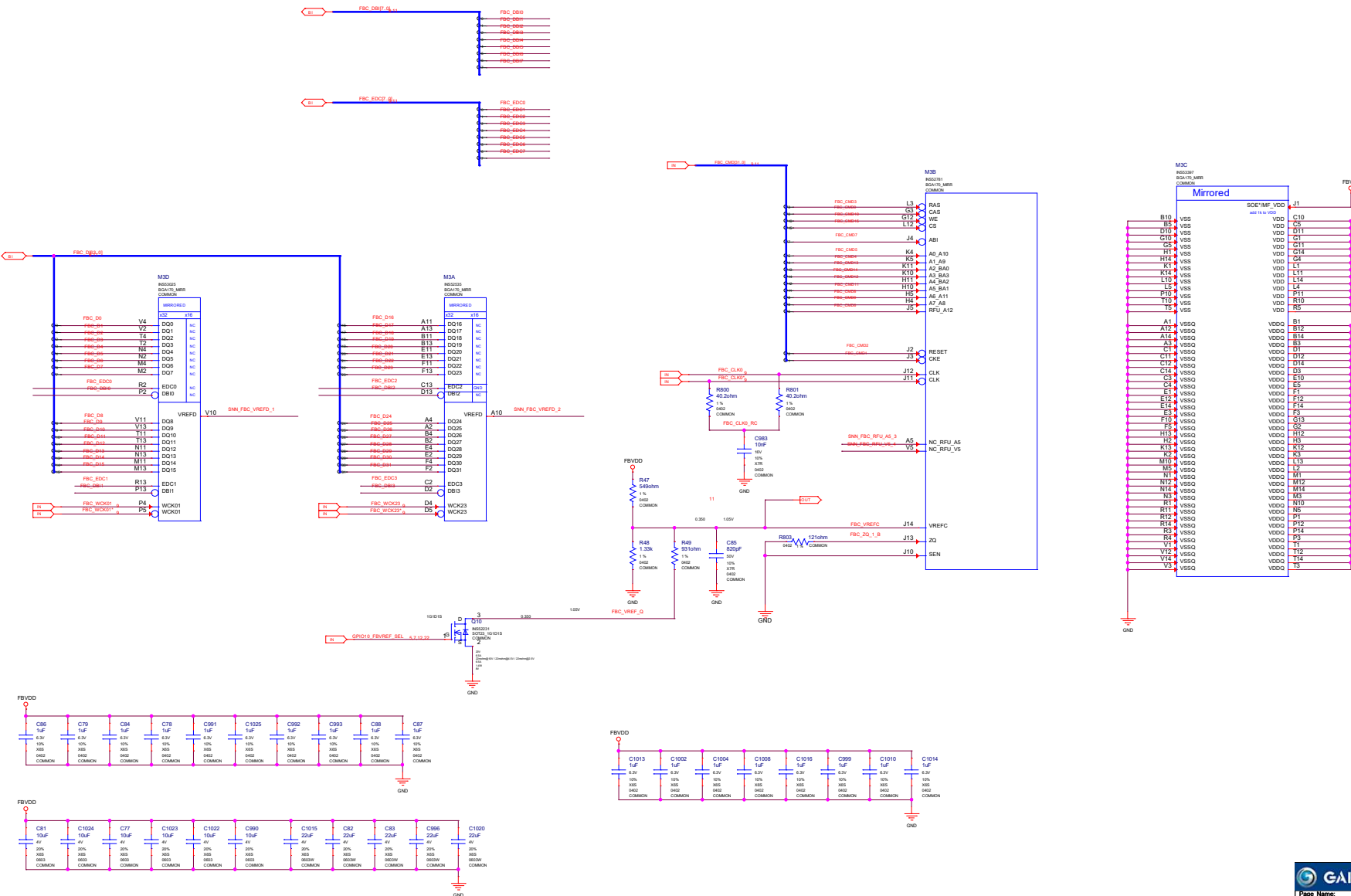


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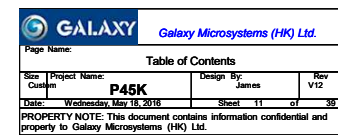


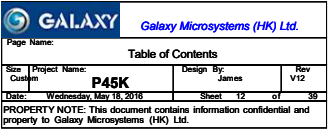


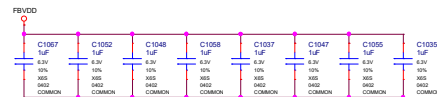
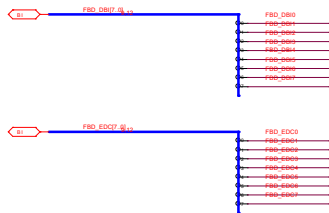
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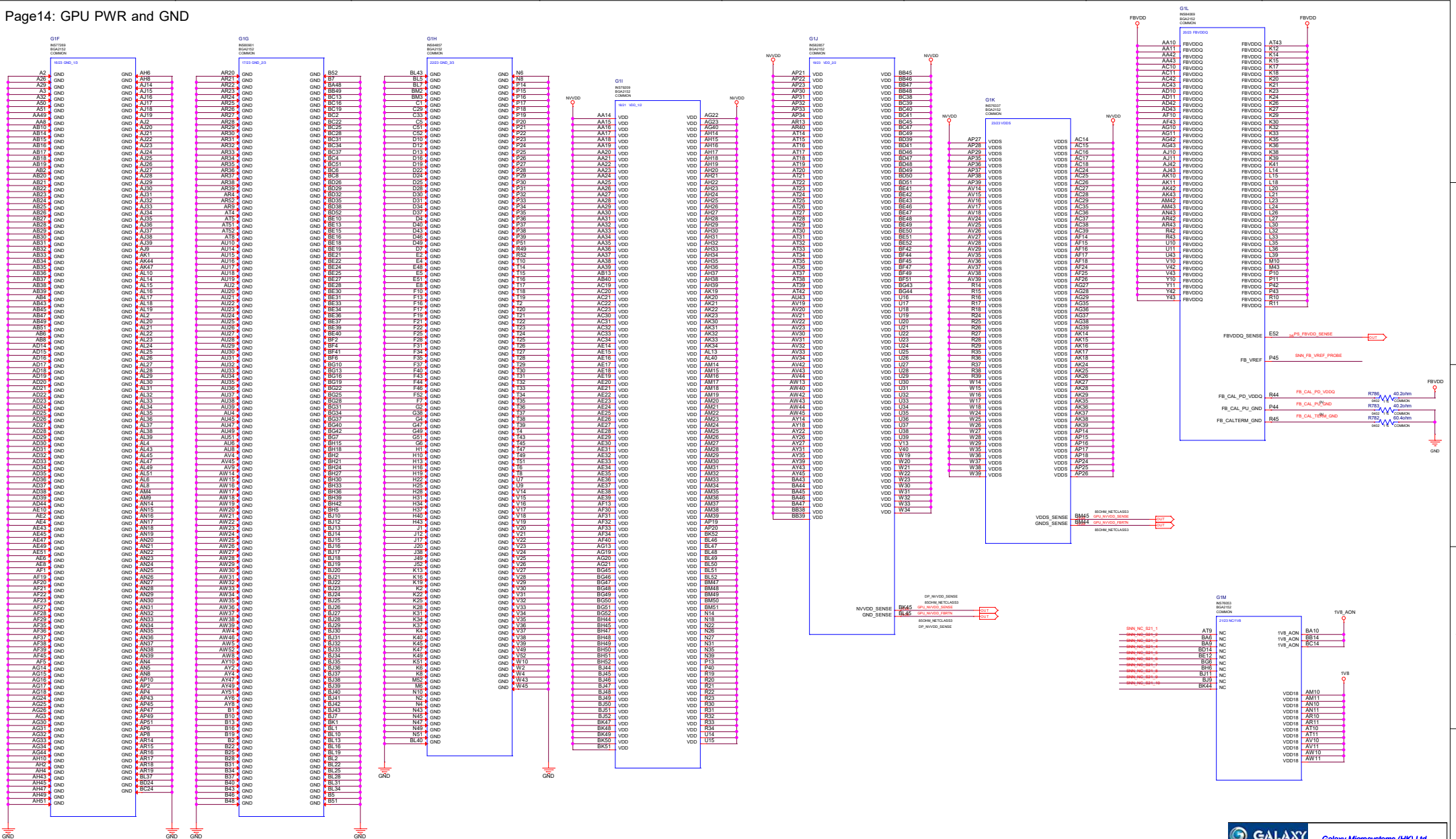
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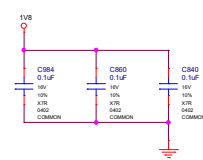
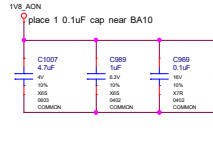
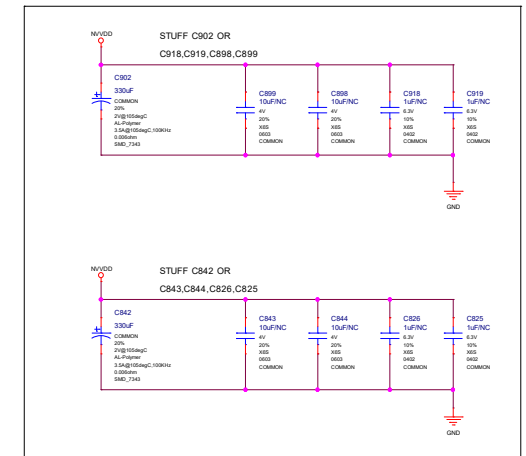
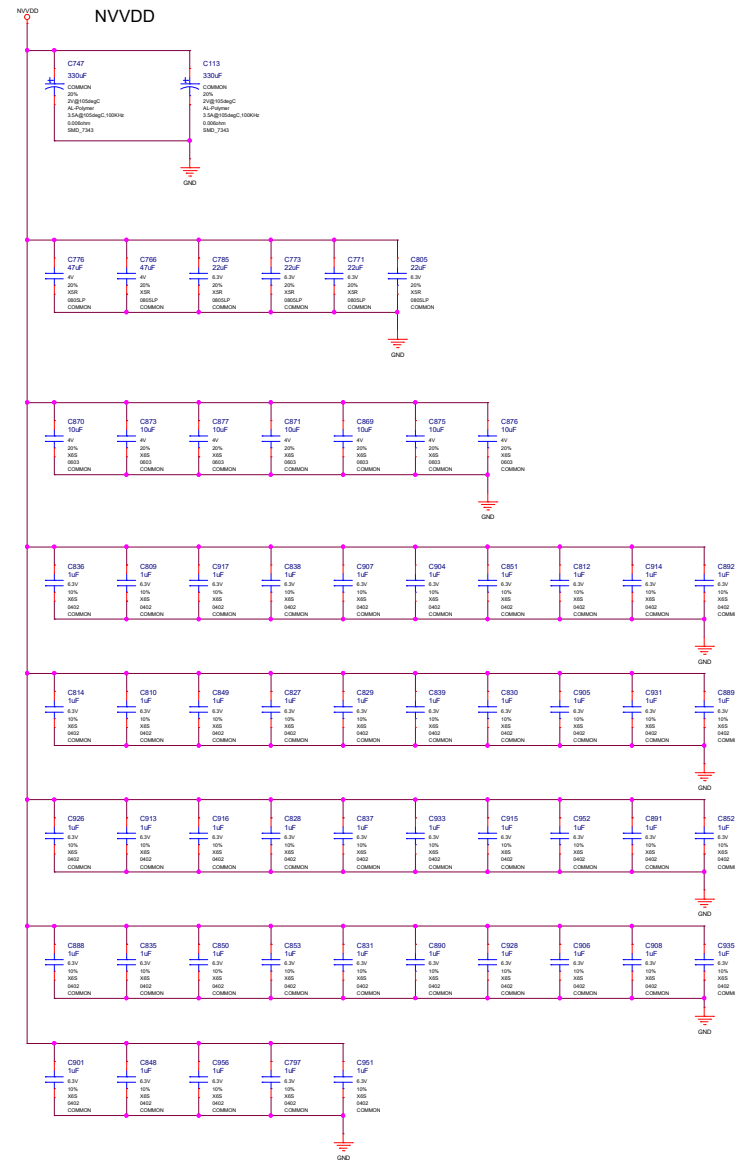





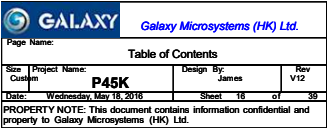


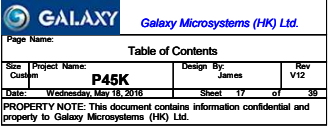
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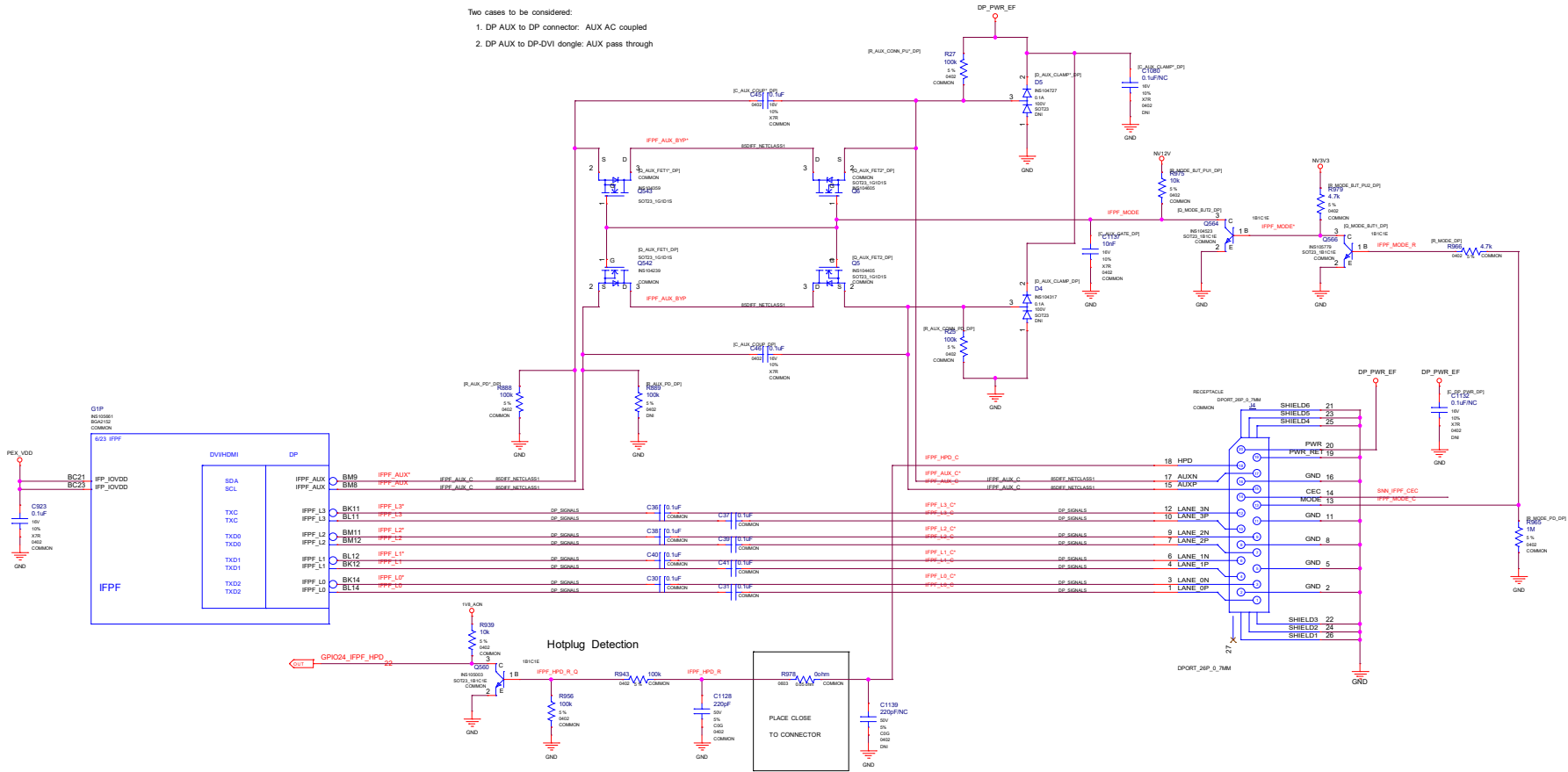


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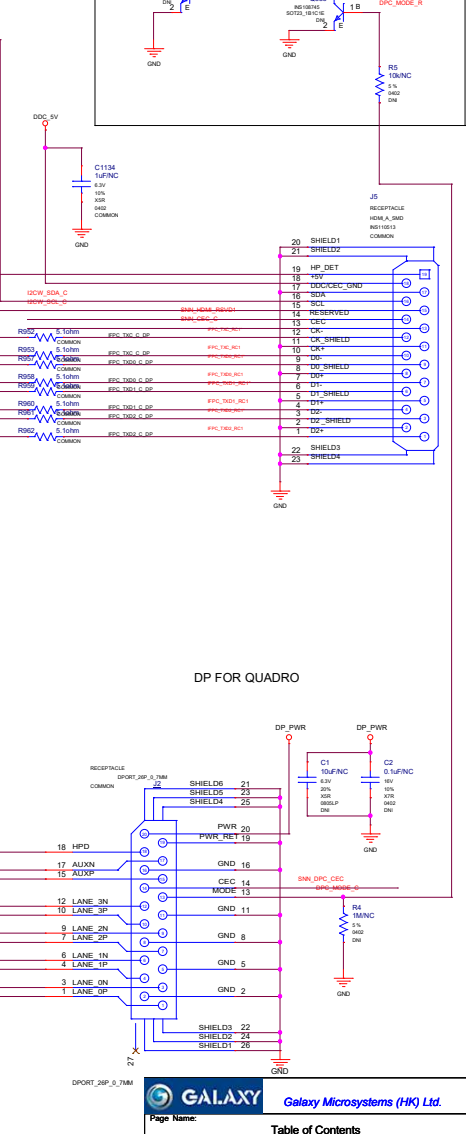
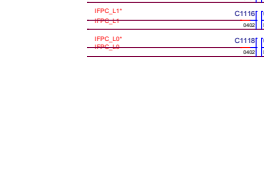
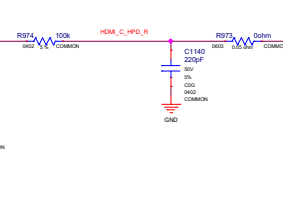
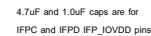
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through




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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IFPF DP

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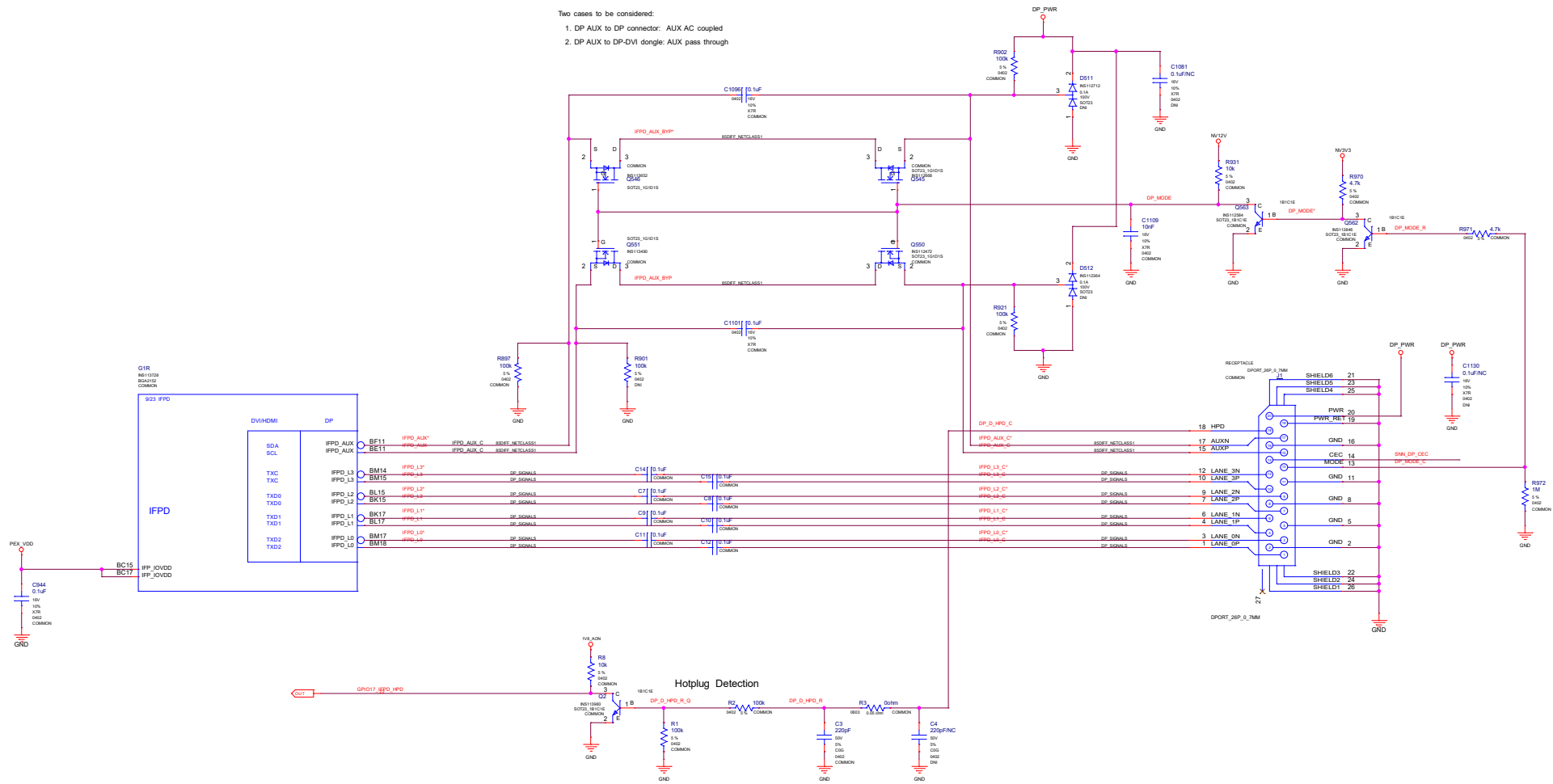
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Two cases to be considered:

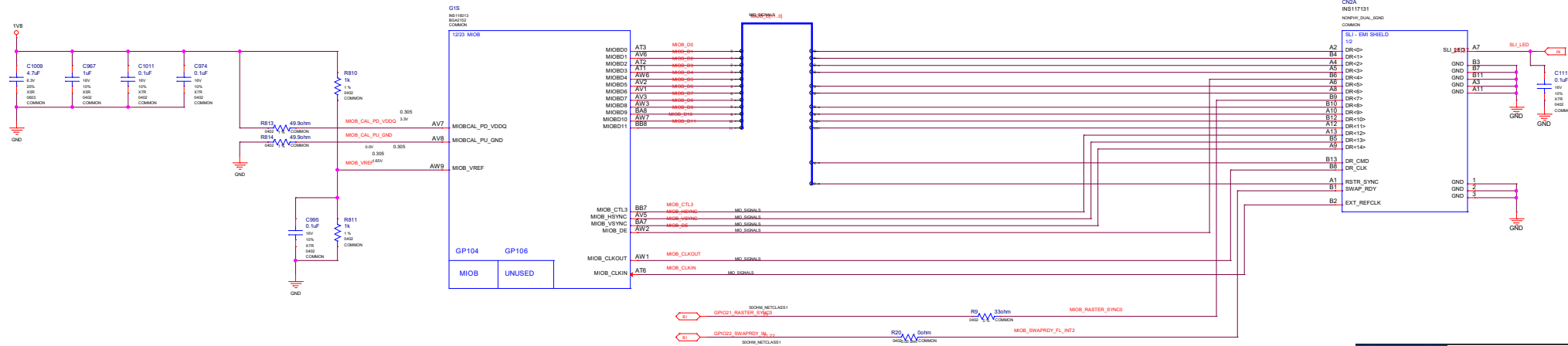
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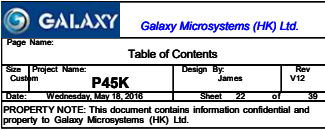
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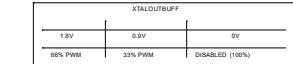
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STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

```
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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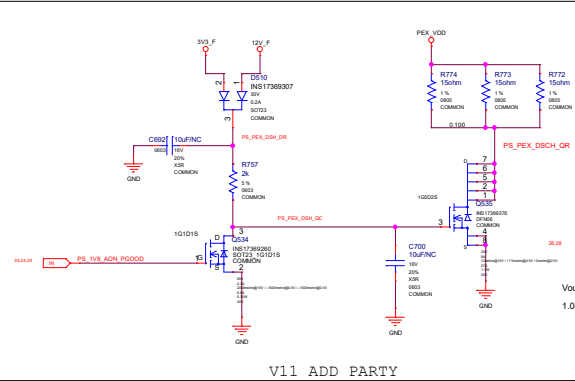
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PS: 1V8, 1V8_AO Galaxy Microsystems (HK) Ltd.

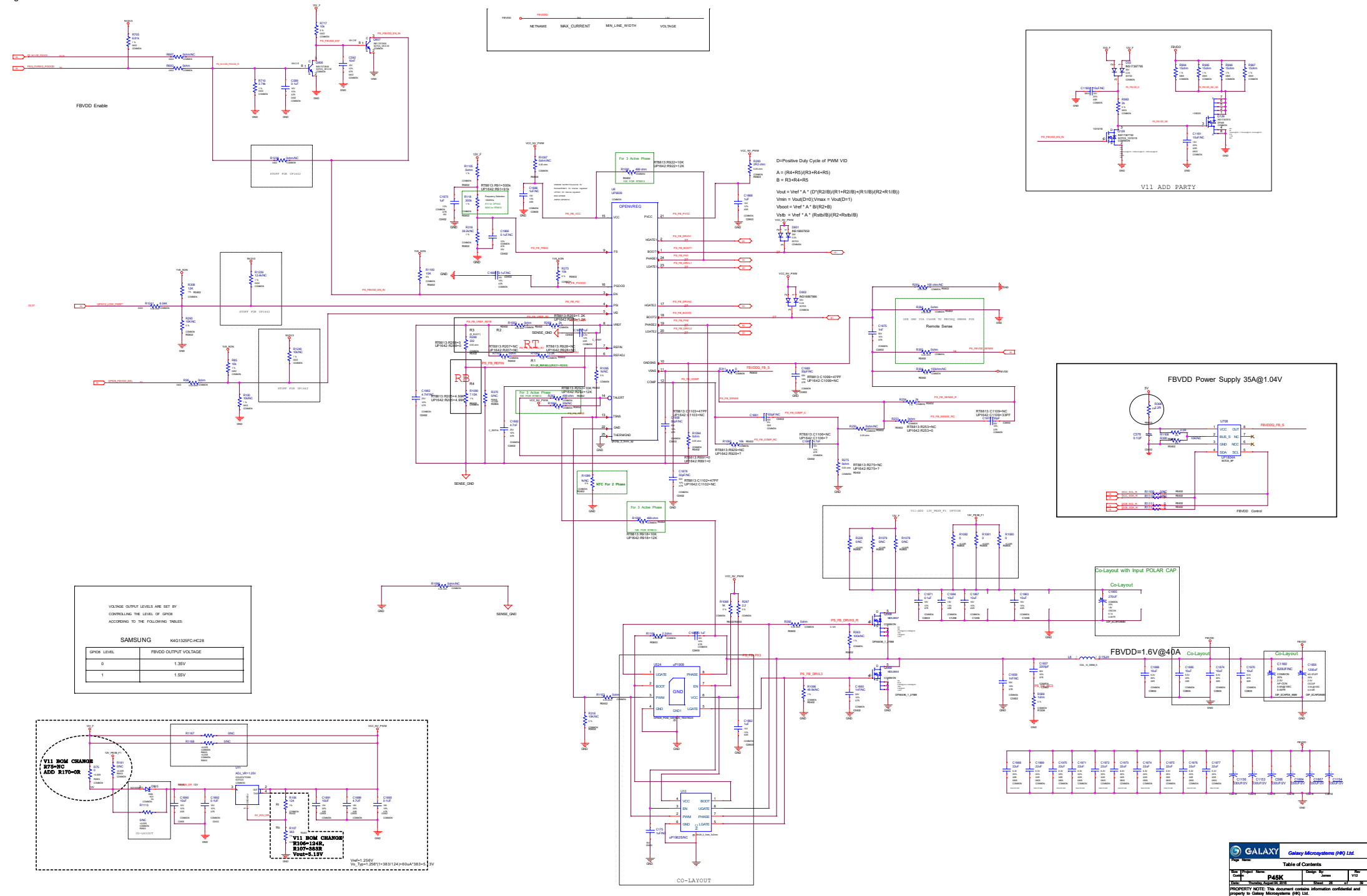
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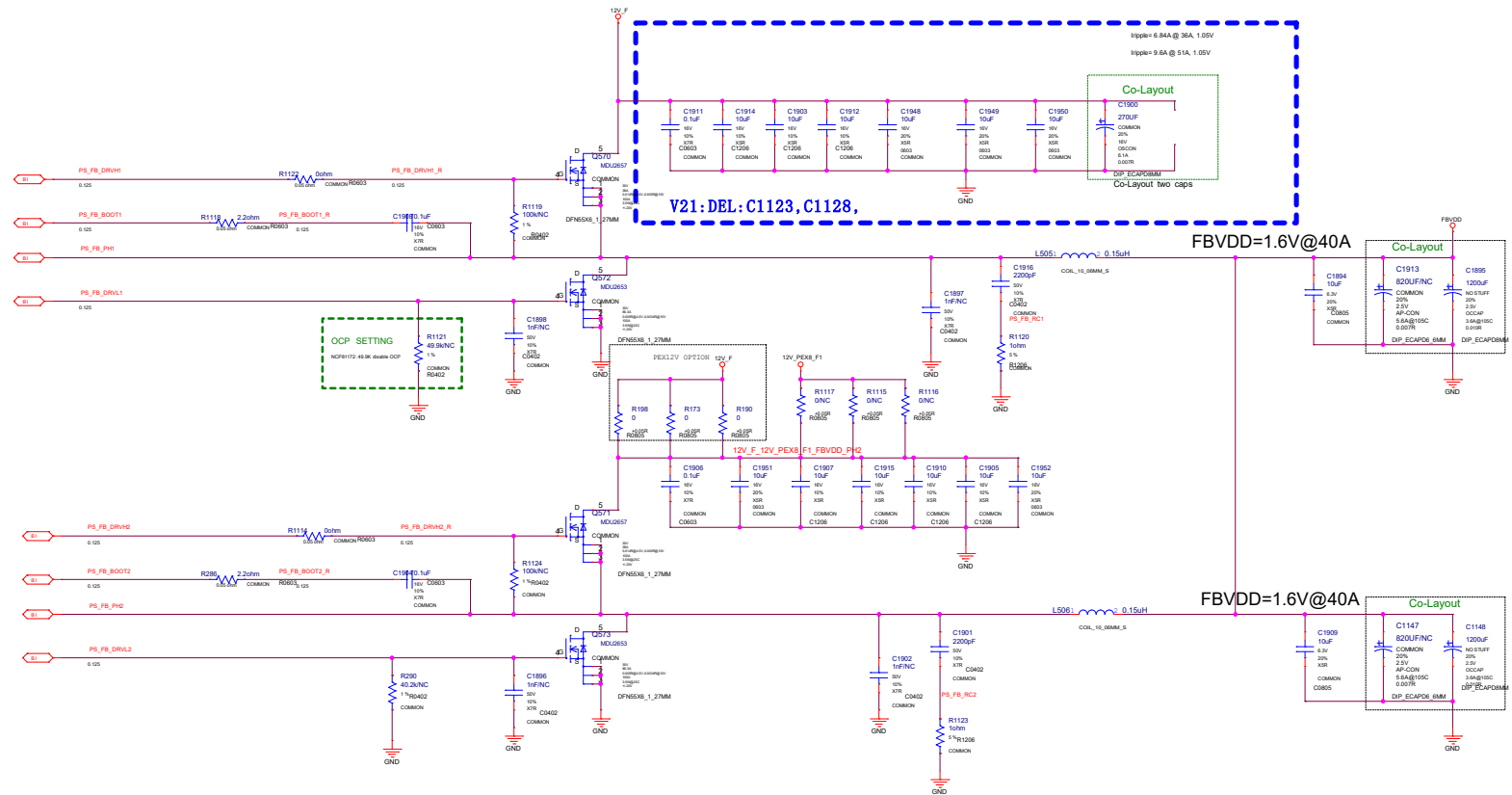
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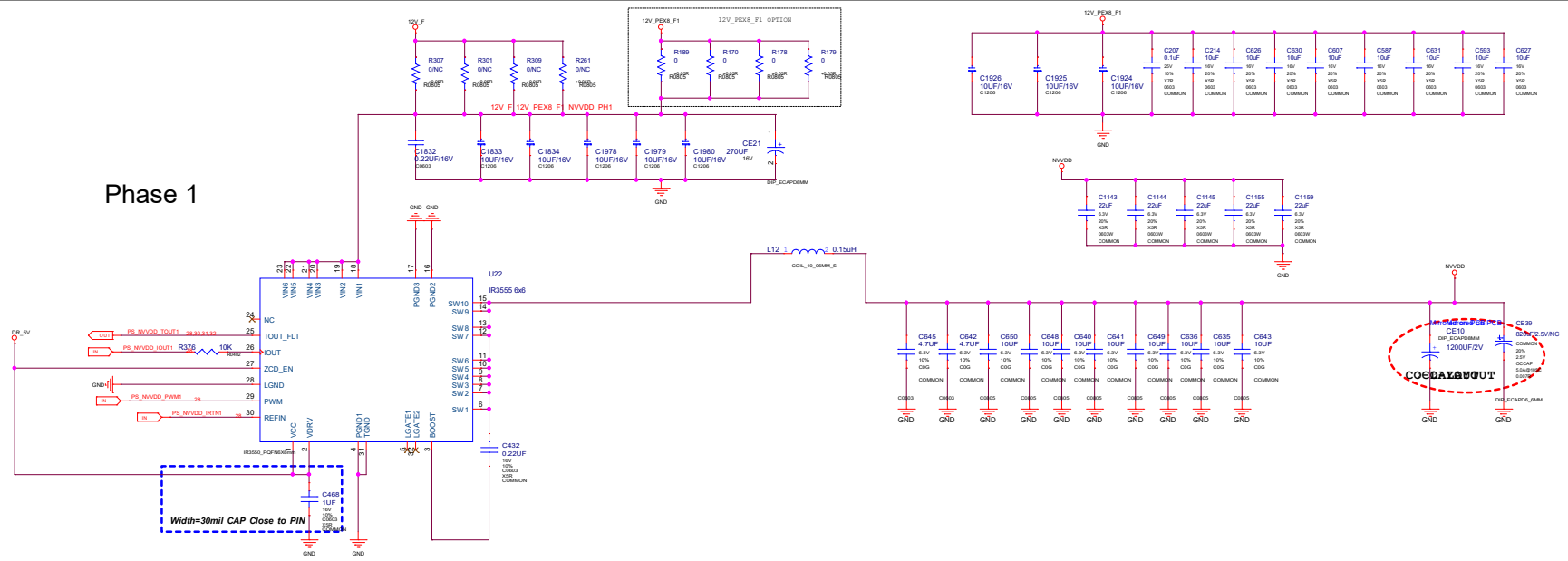




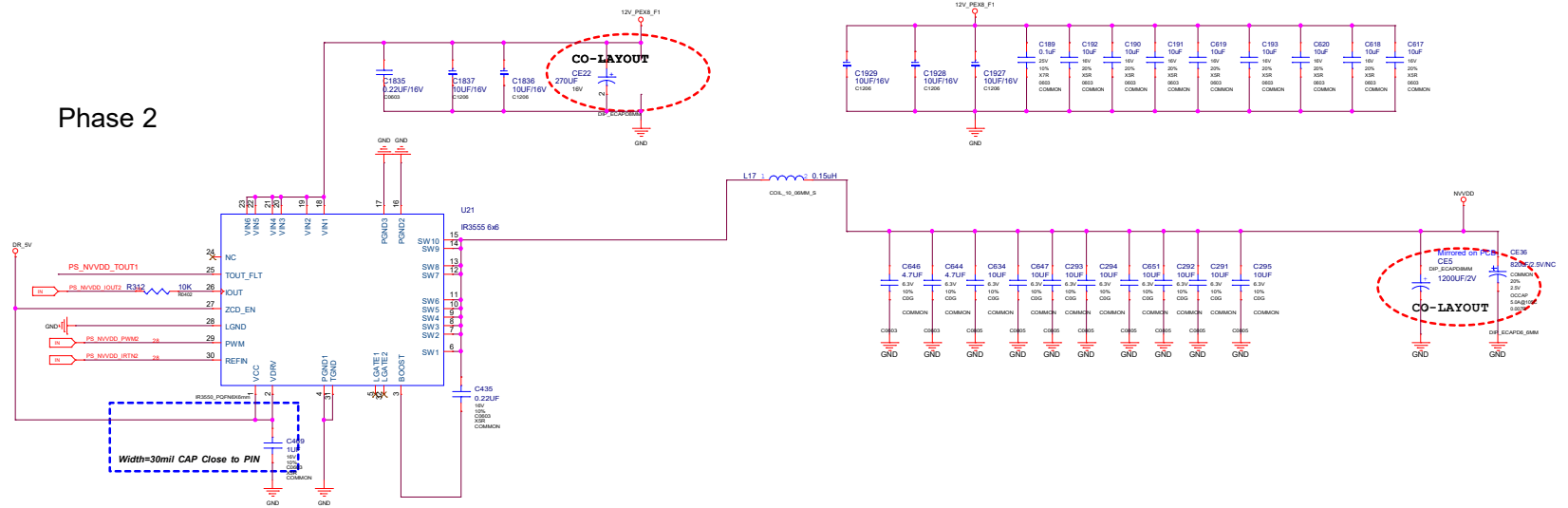
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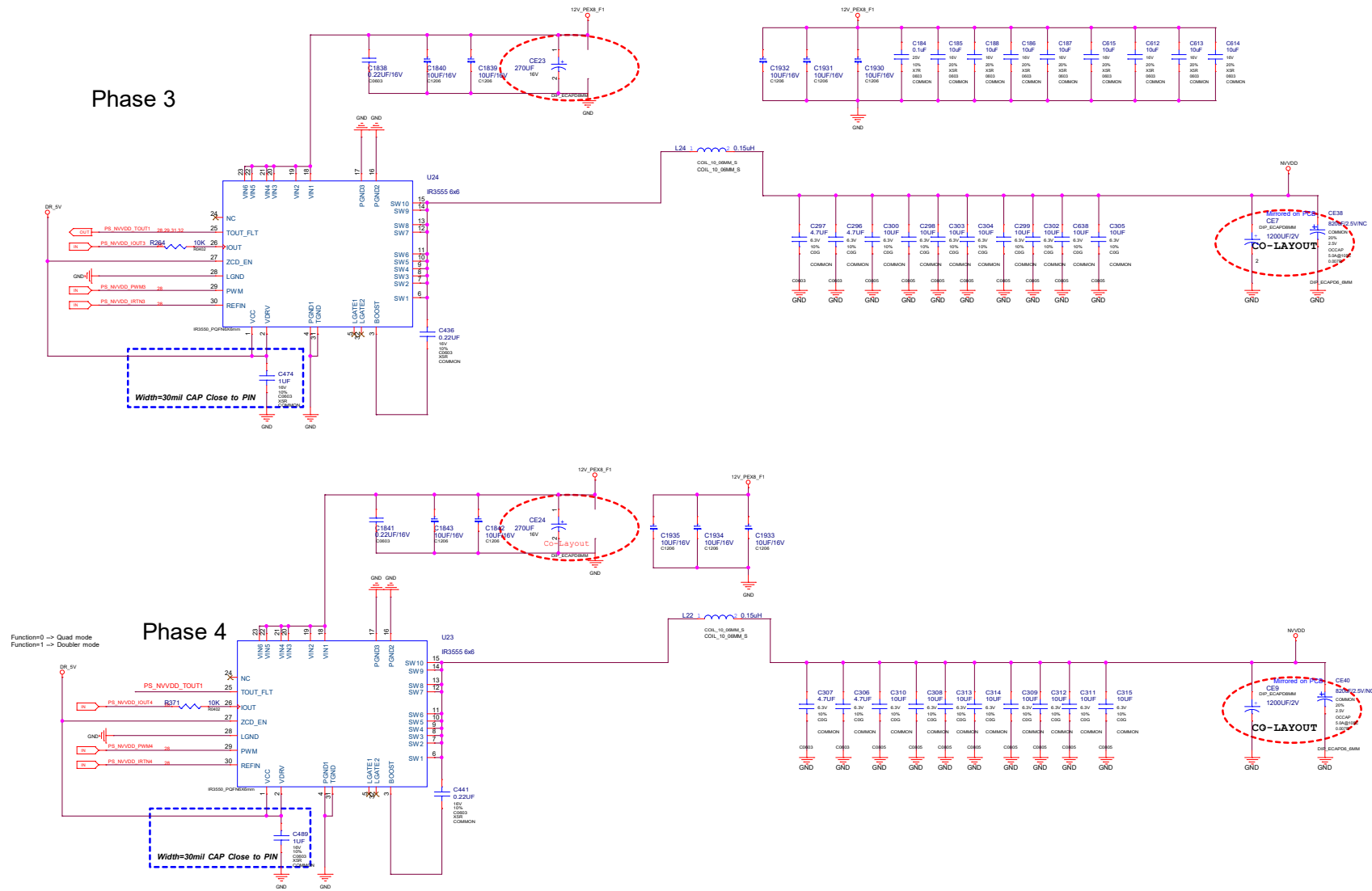
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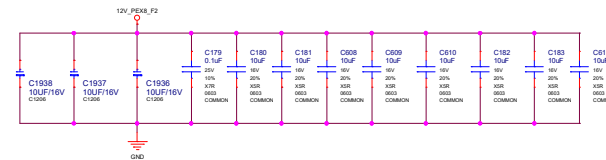
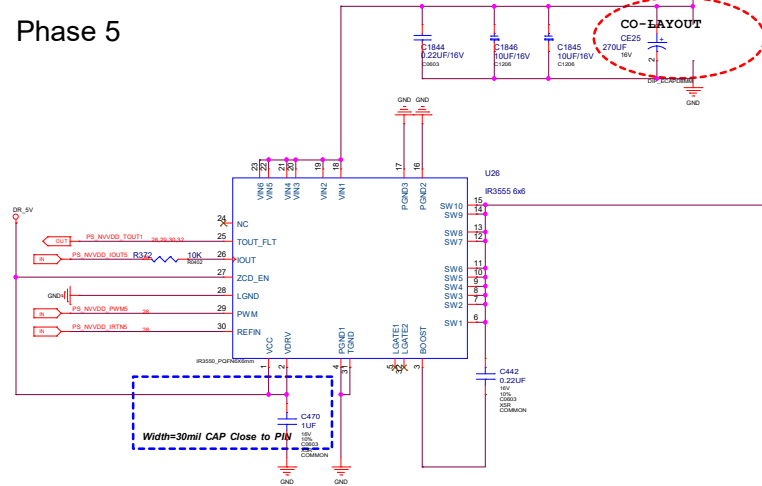


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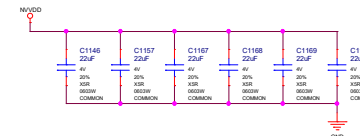
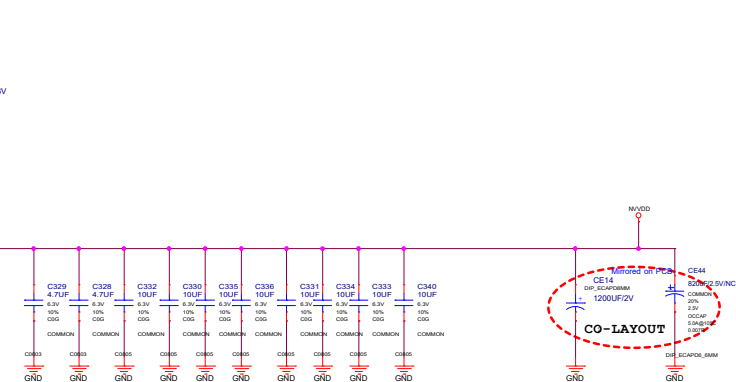
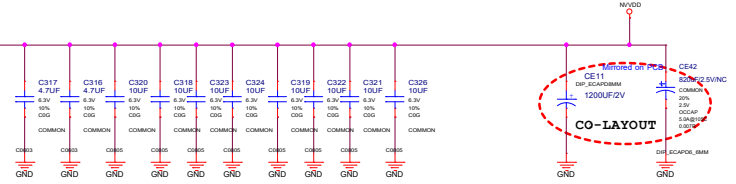
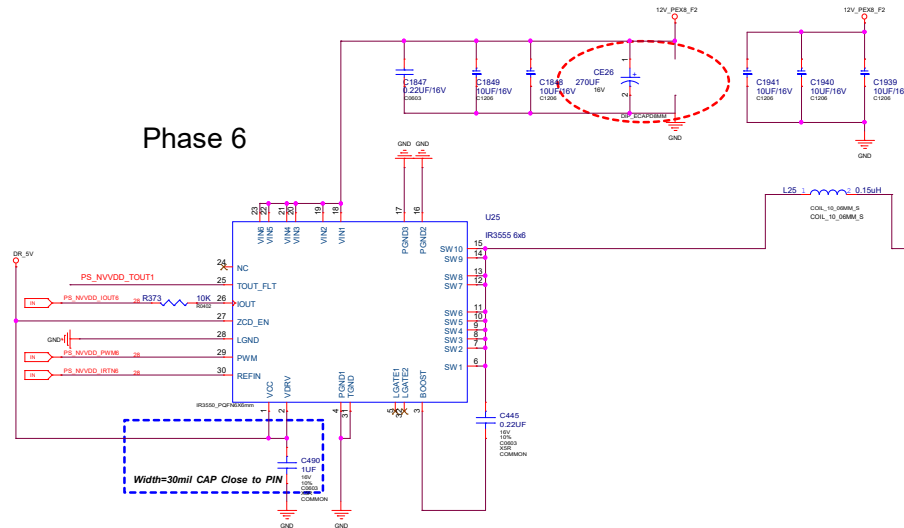


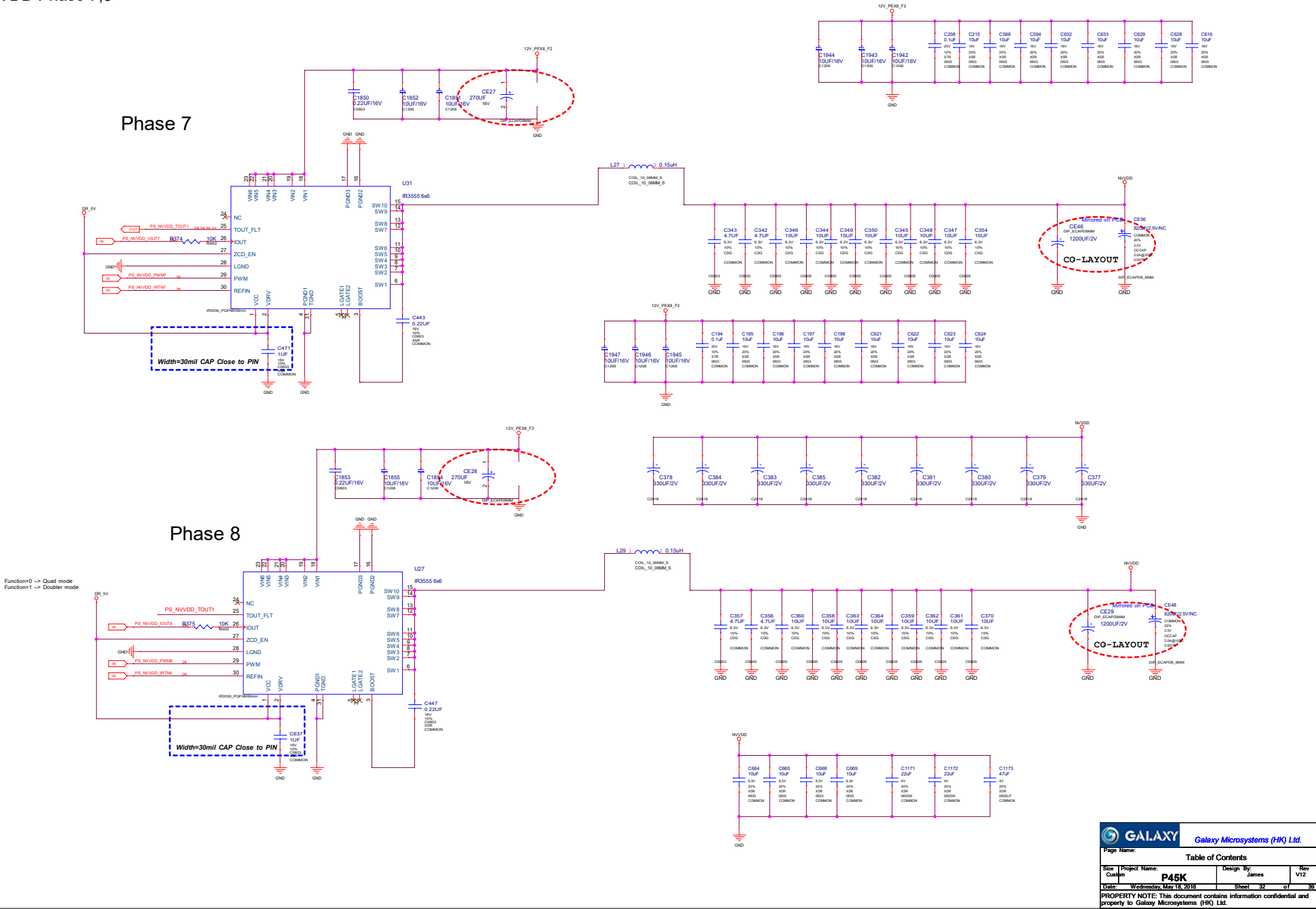
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Phase 6




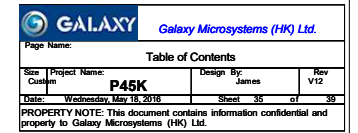
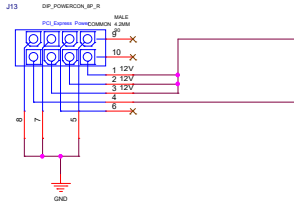


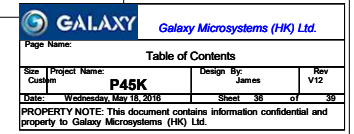


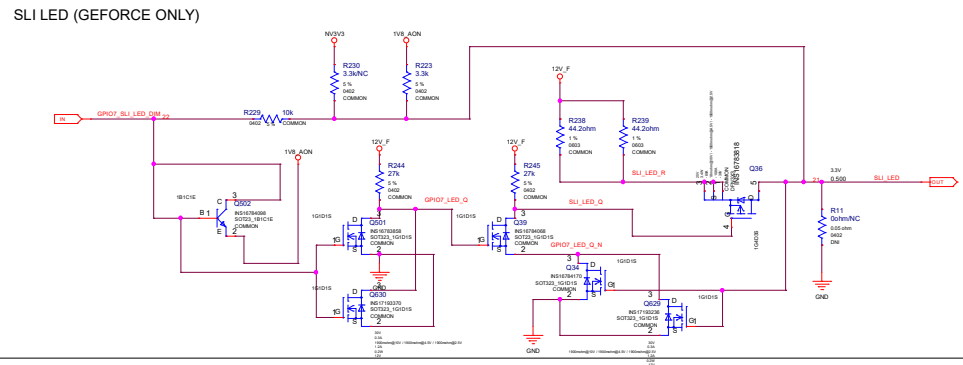
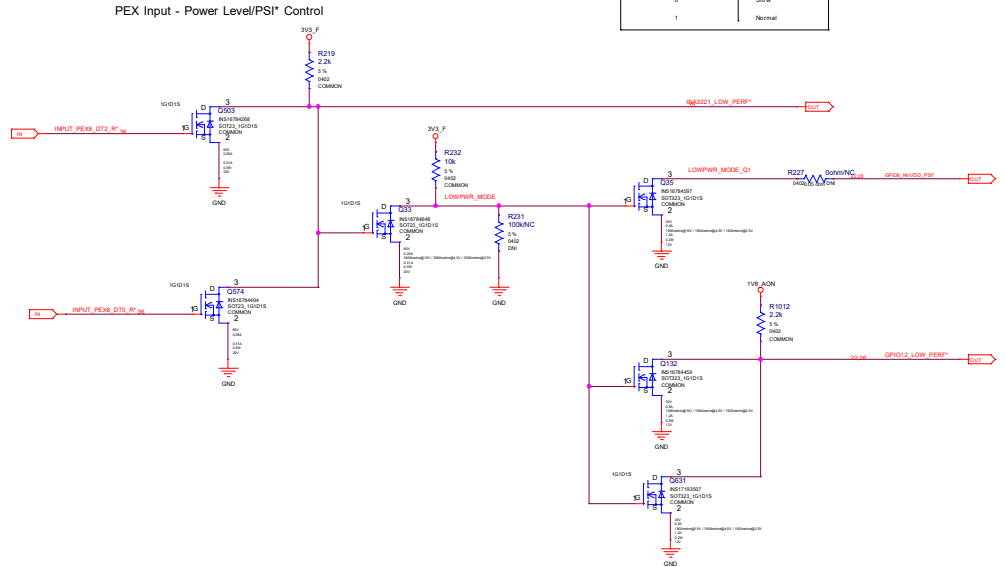
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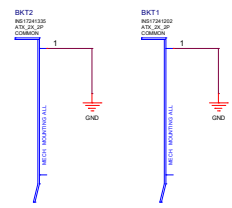




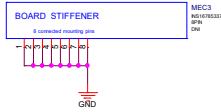


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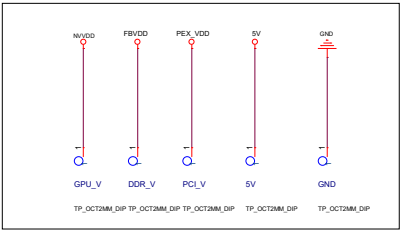
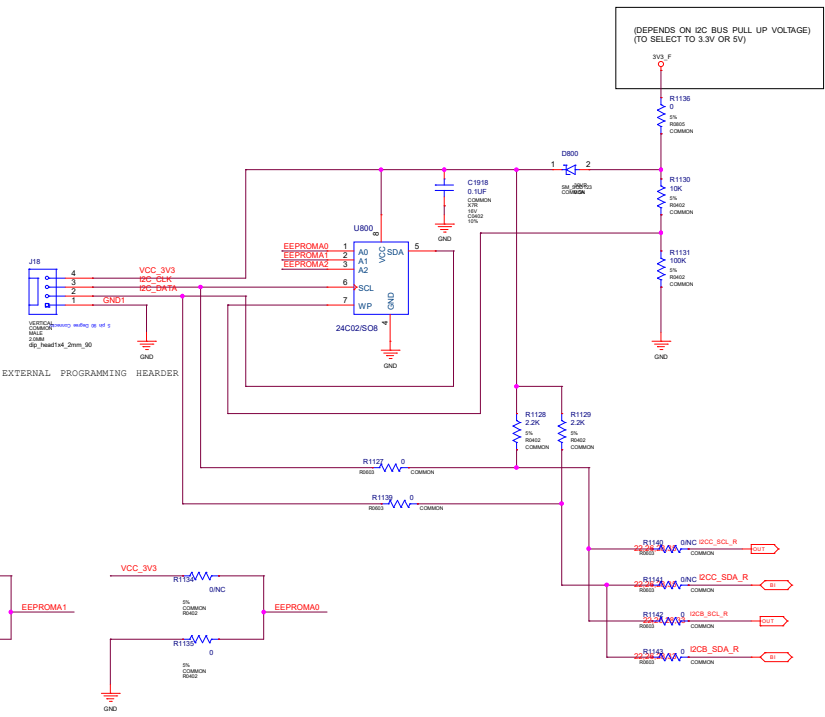
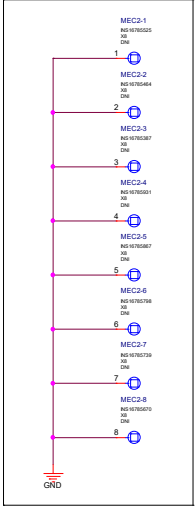
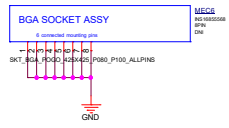
Brackets:



GPU Stiffener



Mechanical Holes Symbol



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V11:

- 1. DP&HDMI PCB Footprint Change to DPORT_26P_0_7MM & HDMI
- 2. Page 33:up to Layout to 0.4-0.5mm line wide
- 3. Page 25 Add S.N.F and PEX CAP
- 4. Add LOADING For FBVDD&PEX_VDD on PAGE 25&26

V12:

- 1. PAGE 33: ADD U702